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09/722,404	11/28/2000	Hidekazu Takata	3917-2	4573

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EXAMINER	
ABRISHAMKAR, KAVEH	
ART UNIT	**PAPER NUMBER**
2131	6

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,404	TAKATA ET AL.	
	Examiner	Art Unit	
	Kaveh Abrishamkar	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to the communication field on November 28, 2000. Claims 1 – 18 were received for consideration. No preliminary amendments for the claims were filed. Currently claims 1 – 18 are being considered.

Information Disclosure Statement

2. A dated and initialed copy of applicant's IDS form 1449, Paper No. 3, is attached to the Office action.

3. The information disclosure statement filed March 21, 2001, Paper No. 3, fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Objections

4. Claims 5 and 13 are objected to because of the following informalities: "comparitor" should be changed to "comparator." Appropriate correction is required.

5. Claim 2, 10 and 15 are objected to because of the following informalities: "an" on should be changed to an "a" before nonvolatile. Appropriate correction is required.

6. Claim 15 is objected to because of the following informalities: there are two periods after the "15." Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 – 18 are rejected under 35 U.S.C. 103(a) as being obvious over Takata (U.S. Patent 6,594,777).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed

in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2). The application being examined deals with a semiconductor storage device with a first store which stores regular data and a dummy data portion, and has a second store which stores the second portion of the regular data to be originally stored in the dummy data portion. The previous application, now U.S. Patent 6,594,777, has a first store that stores regular data but has defective data, which can be replaced with data from the second store that holds a modification data. It would have been obvious to use the dummy data instead of the defective data since both have no useful information, and replace it with a regular data instead of the modification data, to complete the data block.

Regarding claim 1, Takata discloses:

A semiconductor memory device storing regular data and having a security function for preventing unauthorized use of the regular data (column 1 lines 36 – 52), comprising:

a first store including a first storing area for fixedly storing first regular data and a dummy data storing area for fixedly storing dummy data (column 3 lines 45 – 63);

a second store including a second storing area which have a storage capacity equal to at least a storage capacity of the dummy data storing area of the fist storing means and fixedly stores second regular data to be originally stored in the dummy data storing area (Figure 1 item 21B, column 3 lines 40 – 63); and

a read control circuit which compares an input address with the dummy data of an address space of the dummy data storing area, to enable reading of the first regular data from the first store when the input address and the dummy address are not identical, and to disable the reading of the first regular data and enable the reading of the second regular data from the second store when the input address and the dummy address are identical (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced

with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of an "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Regarding claim 7, Takata discloses:

A memory cartridge storing an application program and having a security function for preventing unauthorized use of the application program, comprising:

a first store including a first program storing area for fixedly storing a first application program and a dummy data storing area for fixedly storing dummy data (column 3 lines 45 – 63);

a second store including a second program storing area which have a storage capacity equal to at least a storage capacity of the dummy data storing area of the first store and fixedly stores a second application program to be originally stored in the dummy data storing area (Figure 1 item 21B, column 3 lines 40 – 63); and

a read control circuit which compares an input address with the dummy data of an address space of the dummy data storing area, to enable reading of the first application program from the first store when the input address and the dummy address are not identical, and to disable the reading of the first application program and enable the reading of the second application program from the second store when the input address and the dummy address are identical (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of an "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Regarding claim 8, Takata discloses:

An electronic device for storing an application program and having a security function for preventing unauthorized use of the application program, comprising:

a first store including a first program storing area for fixedly storing a first application program and a dummy data storing area for fixedly storing dummy data (column 3 lines 45 – 63);

a second store including a second program storing area which have a storage capacity equal to at least a storage capacity of the dummy data storing area of the first

store and fixedly stores a second application program to be originally stored in the dummy storage area (Figure 1 item 21B, column 3 lines 40 – 63); and

a read control circuit which compares an input address with the dummy data of an address space of the dummy data storing area, to enable reading of the first application program from the first store when the input address and the dummy address are not identical, and to disable the reading of the first application program and enable the reading of the second application program from the second store when the input address and the dummy address are identical (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of an "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Regarding claim 9, Takata discloses:

A memory cartridge for a game machine storing a game program and having a security function for preventing unauthorized use of the game program, comprising:

a first store including a first program storing area for fixedly storing a first game program and a dummy data storing area for fixedly storing dummy data (column 3 lines 45 – 63);

a second store including a second program storing area which have a storage capacity equal to at least a storage capacity of the dummy data storing area of the first storing means and fixedly stores a second game program to be originally stored in the dummy data storing area (Figure 1 item 21B, column 3 lines 40 – 63); and

a read control circuit which compares an input address with the dummy data of an address space of the dummy data storing area, to enable reading of the first game program from the first store when the input address and the dummy address are not identical, and to disable the reading of the first game program and enable the reading of the second game program from the second store when the input address and the dummy address are identical (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the

proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of a "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Regarding claim 14, Takata discloses:

A method of preventing unauthorized use of regular data stored in a storage device comprising the steps of:

storing in a first storage area first regular data and storing dummy data in a dummy data area of said first storage area (column 3 lines 45 – 63);

storing in a second storage area having a storage capacity equal to at least a storage capacity of the dummy data storing area of the first storage area second regular data to be originally stored in the dummy data storing area (Figure 1 item 21B, column 3 lines 40 – 63); and

comparing an input address with the dummy data of an address space of the dummy data storing area, to enable reading of the first regular data from the first storage area when the input address and the dummy address are not identical, and to

disable the reading of the first regular data and enable the reading of the second regular data from the second storage when the input address and the dummy address are identical (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of a "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Clam 2 is rejected as applied above in rejecting claim 1. Furthermore, Takata discloses:

A semiconductor storage device according to claim 1, wherein the first store includes a masked ROM, and the second store includes a nonvolatile semiconductor memory which is a writable/readable memory (column 3 lines 32 – 39).

Claim 5 is rejected as applied above in rejecting claim 1. Furthermore, Takata discloses:

A semiconductor storage device according to claim 1, wherein the read control circuit includes a comparator for comparing the input address and the dummy address with each other to output a first signal or a second signal, an enabling/disabling circuit for enabling the first store in response to the first signal and disabling the first store in response to the second signal, and a read address output circuit for outputting a read address for the second regular data being stored in the second store in response to the second signal (Figure 2 item 3, column 4 lines 20 – 55).

Claim 10 is rejected as applied above in rejecting claim 9 Furthermore, Takata discloses:

A memory cartridge for a game machine according to claim 9, wherein the first store includes a masked ROM, and the second store includes a nonvolatile semiconductor memory which is a writable/readable memory (column 3 lines 32 – 39).

Claim 13 is rejected as applied above in rejecting claim 9. Furthermore, Takata discloses:

A memory cartridge for a game machine according to claim 9, wherein the read control circuit includes a comparator for comparing the input address and the dummy address with each other to output a first signal or a second signal, an enabling/disabling

circuit for enabling the first store in response to the first signal and disabling the first store in response to the second signal, and a read address output circuit for outputting a read address for the second regular data being stored in the second store in response to the second signal (Figure 2 item 3, column 4 lines 20 – 55).

Claim 15 is rejected as applied above in rejecting claim 14. Furthermore, Takata discloses:

A method according to claim 14, wherein the first storage area resides in a masked ROM, and the second storage area resides in a nonvolatile semiconductor memory which is a writable/readable memory (column 3 lines 32 – 39).

Claim 3 is rejected as applied above in rejecting claim 2. Furthermore, Takata discloses:

A semiconductor storage device according to claim 2, wherein the nonvolatile semiconductor memory has a storage capacity larger than a storage capacity of the second regular data storing area, and further includes a dummy address storing area for storing the dummy address other than the second regular data storing area, and the dummy address to be applied to the read control means is read from the dummy address storing area (column 5 lines 1 – 24).

Claim 6 is rejecting as applied above in rejecting claim 2. Furthermore, Takata discloses:

A semiconductor storage device according to claim 2, wherein the semiconductor nonvolatile memory and the read control circuit is formed within the same single memory chip (column 2 lines 22 – 30).

Claim 11 is rejected as applied above in rejecting claim 10. Furthermore, Takata discloses:

A memory cartridge for a game machine according to claim 10, wherein the nonvolatile semiconductor memory has a storage capacity larger than a storage capacity of the second regular data storing area, and further includes a dummy address storing area for storing the dummy address other than the second regular data storing area, and the dummy address to be applied to the read control circuit is read from the dummy address storing area (column 5 lines 1 – 24).

Claim 16 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, wherein the nonvolatile semiconductor memory has a storage capacity larger than a storage capacity of the second regular data storage area, and further including the step of storing a dummy address in a dummy address storing area, and reading the dummy address from the dummy address storage area (column 5 lines 1 – 24).

Claim 17 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, further including the step of writing to the semiconductor nonvolatile memory with a first write voltage in certain areas, and writing with a second write voltage lower than the first write voltage in other areas (column 5 lines 1 – 13, column 7 lines 47 – 51).

Claim 18 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, further including the steps of comparing the input address and the dummy address with each other to output a first signal or a second signal, and enabling the first storage area in response to the first signal and disabling the first store in response to the second signal, and outputting a read address for the second regular data being stored in the second storage area in response to the second signal (Figure 2 item 3, column 4 lines 20 – 55).

Claim 4 is rejected as applied above in rejecting claim 3. Furthermore, Takata discloses:

A semiconductor storage device according to claim 3, wherein the semiconductor nonvolatile memory is constructed such that the data is written with a first write voltage in the second regular data storing area and the dummy address storing area, and the

data is written with a second write voltage lower than the first write voltage in other areas (column 5 lines 1 – 13, column 7 lines 47 – 51).

Claim 12 is rejected as applied above in rejecting claim 11. Furthermore, Takata discloses:

A memory cartridge for a game machine according to claim 11, wherein the nonvolatile semiconductor is constructed such that the data is written in the second game program storing area and the dummy address storing area with a first write voltage and the data is written with a second write voltage lower than the first write voltage into other areas, in the storing area into which the data is written with the second write voltage, and backup data representing a development of the game obtained by executing the first game program and/or the second game program by a processor of a game machine is written (column 5 lines 1 – 13, column 7 lines 47 – 51).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaveh Abrishamkar whose telephone number is 703-305-8892. The examiner can normally be reached on Monday thru Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 703-305-9648. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

KA
4/24/2004

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
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